

WHAT IS CLAIMED IS:

- 1 1. A method of production testing a video device comprising the steps of:
 2 mounting a device on a test fixture, wherein the test fixture is coupled to a general-
 3 purpose computer;
 4 testing the device using scan techniques, wherein testing the device includes:
 5 serially providing a first test vector to the device;
 6 clocking the device to assert the first test vector within the device;
 7 serially providing a second test vector to the device;
 8 receiving results from the first test vector concurrently with the step of providing
 9 the second test vector; and
 10 comparing the results with expected results.
- 1 2. The method as in Claim 1, wherein the step of testing the device using the scan-test
 2 techniques includes the step of determining, after the step of comparing the results, if the
 3 device has passed a scan-test, wherein the device has passed the scan-test when the
 4 results are equivalent to the expected results and the device has failed the scan-test when
 5 the results are different from the expected results.
- 1 3. The method as in Claim 2, wherein the step of testing the device using the scan-test
 2 techniques further includes the step of placing the device in a good bin when the device
 3 has passed the scan-test.
- 1 4. The method as in Claim 3, wherein the device is taken from the good bin for performing
 2 the step of testing the device using an at speed test.

- 1 5. The method as in Claim 2, wherein the step of testing the device using the scan-test
2 techniques further includes the step of placing the device in a bad bin when the device
3 has failed the scan-test.
- 1 6. The method as in Claim 1, wherein the device is a video processing device.
- 1 7. The method as in Claim 1, wherein the step of serially providing the first test vector to
2 the device includes providing multiple chains of serial test vector values to separate sets
3 of components of the device for concurrently testing the sets of components.
- 1 8. The method as in Claim 1, further including the steps of:
2 selecting one of an at speed test mode and a scan-test mode; and
3 testing the device using an at-speed test when the at speed test mode is selected.
- 1 9. The method as in Claim 8, wherein the device is tested using the scan techniques before
2 the device is tested using the at speed test.
- 1 10. The method as in Claim 1, wherein the general-purpose computer includes one of a
2 peripheral component interconnect port, an accelerated graphics port, a serial port, a
3 JTAG port, or a parallel port for interfacing with the test fixture.

- 1 11. A system comprising:
2 a general purpose computer having:
3 a data processor having an input/output buffer;
4 memory having an input/output buffer coupled to the input/output buffer of the
5 data processor, said memory including a set of instructions to provide a
6 scan-test pattern for testing a device;
7 a communications port having an input/output buffer coupled to the input/output
8 buffer of the data processor;
9 a test fixture having:
10 a communications interface coupled to the communications port, the
11 communications port to receive said scan-test pattern;
12 a scan-chain selector for selecting a particular scan-chain of a plurality of scan
13 chains in said device for testing;
14 a control module to:
15 generate signals to set said device in a scan-test mode;
16 provide said signals to a device socket;
17 load said scan-test pattern, through said device socket, into said particular
18 scan-chain of said device;
19 provide a clock signal to said device socket, wherein said clock is to latch
20 output results from said particular scan-chain;
21 said device socket for interfacing with said device, said device socket to:
22 provide said signals and scan-test pattern from said control module to said
23 particular scan-chain of said device and;
24 receive said output results.

1 12. The system as in Claim 11, wherein said communications port includes a JTAG port.

1 13. The system as in Claim 11, wherein said communications port includes an accelerated
2 graphics port.

- 1 14. The system as in Claim 11, wherein said scan chain selector is configured by a user to
2 select said particular scan chain.
- 1 15. The system as in Claim 11, wherein said scan-chain selector is configured by said set of
2 instructions, through said control module.
- 1 16. The system as in Claim 11, wherein said device includes a graphics processor.

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- 1 17. A test fixture comprising:
2 a bus interface for receiving test signals;
3 a test mode selector coupled to the bus interface, said test mode selector to route said test
4 signals from said bus interface to one of an at-speed operating path and a scan-test
5 path;
6 a scan-test control module coupled to said scan-test path of said test mode selector, said
7 scan-test control module to:
8 engage a scan-test mode in a device;
9 selecting a particular scan-chain of a plurality of scan-chains associated with said
10 device;
11 providing a scan pattern to a test socket, wherein said scan pattern is loaded into
12 said scan-chain;
13 receiving results from said device, wherein results are related to said scan pattern;
14 a test socket having:
15 a first input/output buffer coupled to said at-speed operating path of said test
16 mode selector;
17 a second input/output buffer coupled to said scan-test path of said test mode
18 selector; and
19 a third input/output buffer coupled buffer coupled to said device.
- 1 18. The test fixture as in Claim 17, wherein said bus interface includes an accelerated
2 graphics port interface.
- 1 19. The test fixture as in Claim 17, wherein said bus interface is coupled to a bus port of an
2 information handling system.
- 1 20. The test fixture as in Claim 17, wherein the test mode selector is configured through said
2 test signals to select from one of the at-speed operating path and the scan-test path.

1 21. The test fixture as in Claim 17, wherein the at-speed operating path is used to provide test
2 signals associated with at-speed tests.

1 22. The test fixture as in Claim 17, wherein said device includes a graphics processor.

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